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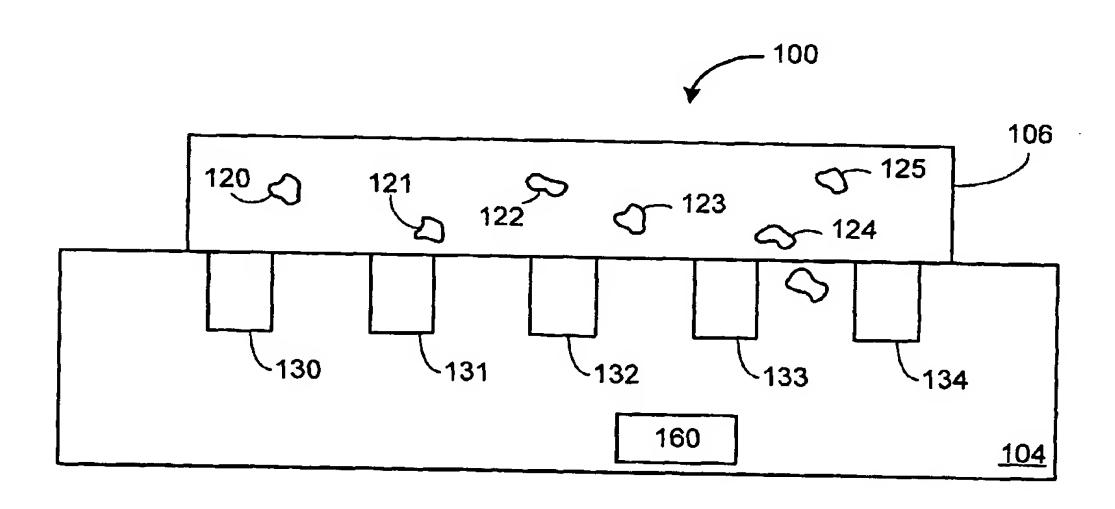
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[Continued on next page]

(54) Title: TAMPER-RESISTANT PACKAGING AND APPROACH



(57) Abstract: A tamper-resistant packaging approach protects non-volatile memory (108). According to an example embodiment of the present invention, a package (106) having a plurality of magnetic particles (120-125) therein is arranged with an integrated circuit device (100) to cause a plurality of magnetically-responsive circuit nodes (130-134) to take on magnetic states. Each magnetic state is detected as a logic state, and then compared with a real-time logic state of the magnetically-responsive circuit nodes and, in response to a stored logic state being different from a real-time logic state, package tampering is detected. In one instance, tampering is detected when the magnetic state of one of the magnetically-responsive circuit nodes is altered as a portion of the package is removed. The detected tampering may alter a characteristic of the integrated circuit, such as by altering stored data or setting a tamper flag that indicates the package has been tampered with.



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Category °	Citation of document with indicate	
	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 278 (P-322), 19 December 1984 (1984-12-19) & JP 59 144094 A (HITACHI SEISAKUSHO KK), 17 August 1984 (1984-08-17) abstract	1,15,19
	US 2001/033012 A1 (K0EMMERLING OLIVER ET AL) 25 October 2001 (2001-10-25) paragraph '0097! - paragraph '0117! paragraph '0218! - paragraph '0219!	1,15,19 2,8-14, 16-19
	US 2002/008988 A1 (LENSSEN KARS-MICHIEL HUBERT ET AL) 24 January 2002 (2002-01-24) the whole document	1-20

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Date of the actual completion of the international search	Date of mailing of the international search report
10 February 2005	21/02/2005
lame and mailing address of the ISA  European Patent Office, P.B. 5818 Patentlaan 2  NL – 2280 HV Rijswijk	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT Category ° Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No. A PATENT ABSTRACTS OF JAPAN 1-20 vol. 009, no. 093 (P-351), 23 April 1985 (1985-04-23) & JP 59 221631 A (FUJITSU KK), 13 December 1984 (1984-12-13) abstract

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